Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 4. This sheet 4/4, which includes Fig. 4, replaces the original sheet including Fig.4. In Figure 4, the designation "(Prior Art)" has been added.

Attachment: *Replacement Sheet*

REMARKS

The claims have been amended by rewriting claims 2, 5, 8, 10-12, and 16. Claims 1-19 remain in the application.

Applicants respectfully request that the rejection of the claims presented be reconsidered and withdrawn in light of the amendments above and/or the discussion which follows and that the application be found in condition for immediate allowance.

The 35 USC §112 Rejections

Claims 2 and 5-18 stand rejected under 35 USC 112, second paragraph, as being indefinite for failing to particular point out and distinctly claim subject matter which Applicants regard as the invention.

Applicants acknowledge with appreciation the comments of the Examiner in the Official Action. The amendments made hereinabove are intended to correct the deficiency of the claims amended under 35 USC 112 and to bring the application into condition for immediate allowance, which is respectfully solicited. Each rejection is specifically addressed below.

Claim 2

Claim 2 stands rejected specifically because it is not clear to the Examiner what is meant by

"after said second data input/output circuit outputs said data taken thereinto to said data bus, said second data input/output circuit outputs said data thereof to said data bus."

The Examiner asks for clarification as to whether this phrase represents that data is output twice on the data bus or is different data being output to the bus.

In direct response to the Examiner's query, it is different data which is being output to the bus.

Applicants fully concur with the Examiner's assertion of ambiguity and attribute it to improper use of the word "said," which clearly does not belong since there is no antecedent basis for "data thereof."

In response to the rejection, Applicants have amended claim 2 in an attempt to remove any ambiguity. "Said data thereof" has been amended to read "data thereof." As such, "data thereof" is newly introduced at that point in the claims and *prima facie* refers to data which is other than the "data taken" which was first introduced in claim 1.

Applicants could have used terms such as first data and second data and instead elected to be more descriptive and therefore chose "data taken" and "data thereof." These are two distinctly different data. "Data taken" refers to data received from the first input/output circuit. "Data thereof" refers to other data and is specified to be data thereof the second input/output circuit. This is well supported in the specification in at least the sections describing periods (c) and (g) of Fig. 2 beginning at paragraph [0063].

Therefore, regarding claim 2, Applicants believe the amendment to claim 2 and

the preceding discussion should be sufficient to overcome the Examiner's rejection, at least on the basis of 35 USC 112 paragraph 2.

Claims 5 and 6-10

Claims 5 and 6-10 stand rejected for lacking antecedent basis for "said read instruction" on line 20.

In response, "said read instruction" has been amended to read "a read instruction." Applicants believe this amendment should be sufficient to overcome this particular rejection.

Claims 6-10 stand rejected because they depend on claim for 5 and seeing as to how the rejection of claim 5 has been addressed, the rejection of claims 6-10 is likewise believed to be overcome for the same reason.

Claims 6 also stands rejected for lacking antecedent basis for "the read instruction" on line 2.

In response, Applicants believe no amendment to claim 6 is needed in this regard because antecedent basis for "read instruction" is now provided in claim 5, from which claim 6 draws dependency, as amended to read "a read instruction."

Claim 8 is also rejected for lacking antecedent basis of "the write instruction" on line 2 and "the outside" on line 5.

In response, regarding the write-instruction rejection, "the write instruction" has been amended to read "a write instruction." Applicants believe this amendment should be sufficient to overcome this particular rejection.

Regarding "the outside" rejection on line 5, Applicants have removed the language which previous to the amendment read "said write data being transferred from the outside." Applicants believe this amendment resolves the issue. Note that Applicants have voluntarily made the same amendment to claim 10 for similar language contained therein.

Claims 11 and 12-15

Claim 11 stands rejected for lacking positive antecedent basis for "said output buffer" on line 10.

In response, Applicants have amended claim 11 so as to change "output buffer" to "first buffer." In looking closely to the language of claim 11, Applicants note that it is the first buffer that outputs. Thus, Applicants believe this provides *prima facie* support for the amendment.

Claims and 12-15 stand rejected because they depend on claim 11. As the deficiency of claim 11 has been addressed, Applicants assert that these claims are in condition for allowance for the same reasons.

Claim 12 is additionally rejected based on lack of positive antecedent basis of "the data input/output circuit" on line 1.

Claims 16-18

Claims 16 stands rejected for lacking antecedent basis for "said first input/output circuit" on lines 2 and 3; and for lacking antecedent basis for "said second data input/output circuit" on lines 4-5 and 6.

In response, Applicants have rewritten claims 16 so that the word "said" now reads "a" in both cases. Applicants believe this resolves the issues surrounding this rejection and respectfully requests that the claim be passed to issuance.

Claims 17 and 18 stand rejected on the same basis and seeing as to how this issue has been resolved in claim 16, from which claims 17 and 18 depend, Applicants believe these claims are in condition for allowance as well, without amendment.

The 35 USC §102 Rejections

Claims 1-4 stand rejected as anticipated by the disclosure of Walker in United States Patent 6,127,849, (hereinafter "Walker"). Applicants respectfully request consideration of the below arguments for patentability and reconsideration and withdrawal of the rejection.

The Walker reference

The undersigned spent a number of years designing analog integrated circuits and bus drivers for digital VLSI circuits and finds the disclosure of Walker to be fascinating. The circuits shown in Fig. 4a and cited by the Examiner allows for the simultaneous transmission of data in two directions on a single capacitively loaded line referred to as DBUS 404. Output drivers 406a and 406b, by design, oppose each other on the bus. As a result, when output drivers 406a and 406b are driving opposing data, the result is a mid-level voltage Vmid on DBUS 404. Yet, even with this

contention on DBUS 404, as shown in Fig. 4b, the data at Dout1 properly follows the data on Din2, and likewise, the data on Dout2 follows the data on Din1.

Referring now to Walker's Fig. 3a, this feat is accomplished by placing a comparator 320 which senses at 316 the voltage level on DBUS 404 and which compares this voltage against a reference 328. Reference 328 in turn is switched between two references Vref1 and Vref2 which lie just above and below the midlevel voltage Vmid. Even though what is being detected is Din2 across DBUS 404, whether Vref1 or Vref2 is switched-in depends on what is happening on in the near side of DBUS 404. Specifically, the depends on the value of Din 304. The changing of comparator references between Vref1 and Vref2 would cause a glitch at Dout 332 if it were not for transition detector 314 and snubbing FET N307 which effectively suppress the glitch.

thus
Bus, with the technology disclosed by Walker, it is possible to maintain a full-time simultaneous connection between Din2 and Dout1, and Din1 and Dout2.

The simultaneous, always on, connection is implied in the title of Walker, and is spelled out explicitly in the background section to which the circuit relates. Specifically, column 1, lines 36 through 43, of Walker's background section states:

> One approach to increasing data bandwidth without expanding bus size is to use simultaneous bidirectional I/O circuits. In systems having simultaneous bidirectional I/O circuits, data can be transmitted and received on the same data bus line at the same time. This allows the data bandwidth to be essentially doubled without increasing the bus size.

How the claim language distinguishes over Walker

Contradistinctively, Applicants invention relates to clocked synchronous circuits in which data contention between output drivers is to be avoided, and if not avoided, would cause contending output drivers to fry. With clocked synchronous circuits, output drivers are carefully timed using a common clock line and output enable (OE) lines on each driver to successively switch from one driver to another. It is this successive switching which avoids contention that distinguishes over Walker since, in Walker, the output drivers simultaneously drive the bus and there is never any need to successively switch drivers.

Claim 1

This limitation is expressly recited in the following bold-highlighted portions of Applicants' claim 1:

> 1. Apparatus comprising:
>
> first and second data input/output circuits, each of said circuits receiving data output from the other and releasing data stored therein; and
>
> a data bus transferring data between said first and second data input/output circuits,
>
> wherein, upon data output being **successively switched from said first data input/output circuit to said second data input/output circuit,** said second data input/output circuit takes in data output from said first data input/output circuit and releases said data taken thereinto to said data bus.

Therefore, Applicants respectfully submit that the rejection made in the Official Action is in error.

It is Applicants' understanding that a rejection on the basis of anticipation under 35 USC 102 is appropriate where each element of a claim at issue is found in a single prior art reference. See Kalman v Kimberly-Clark Corp., 218 USPQ 781 at 789, (Fed. Cir. 1983). The requirement is for an element by element comparison, including all limitations, of the recited structure, function and operative steps with what is found in the reference sought to be applied. The rejection is proper where such an element by element comparison finds identity for each element/limitation within the four corners of the reference.

It is respectfully submitted that the rejection made in the Official Action falls short of this standard. Further, it is respectfully submitted that no rejection can be framed on the basis of the references cited, whether applied or not, which will support a refusal to allow the claims as presented, without regard for whether that possible rejection is grounded on anticipation under 35 USC 102 or obviousness under 35 USC 103.

The simultaneous / always-on nature of Walker's circuits is categorically in opposition to Applicants successively switched circuits. Further, at least the above bold-highlighted language clearly distinguishes over Walker such that claim 1 does not read on Walker. Should the Examiner disagree, it is respectfully requested that the Examiner provide specific pointers in the Walker reference for a teaching of successively switching from a first data input/output circuit to a second data input/output circuit.

Further, Walker also fails to find identity with the following bold highlighted limitations of claim 1:

1. Apparatus comprising:

first and second data input/output circuits, each of said circuits receiving data output from the other and releasing data stored therein; and

a data bus transferring data between said first and second data input/output circuits,

wherein, upon data output being successively switched from said first data input/output circuit to said second data input/output circuit, **said second data input/output circuit takes in data output from said first data input/output circuit and releases said data taken thereInto to said data bus.**

Walker fails to meet this limitation, notwithstanding the Examiner's recitation of column 8, line 47 through column 9, line 65, because, in order to meet this limitation, the data would have to be released from one driver would have to be the data released from the other driver. Whereas, in Walker, there is only disclosure for releasing Din. See, for example, Walker's figure 3a wherein the value to be driven onto the DBUS 404 at pin 316 depends only on the value of Din 304 (and nothing else).

Should the Examiner disagree, it is respectfully requested that the Examiner provide specific pointers to the location in the references of a teaching of a second data input/output circuit releasing, to a data bus, data taken thereinto from a first data input/output circuit.

Even if one were to take to more liberal view that the Walker patent might be a reference for an obviousness rejection, support necessary for such a rejection is absent from the Official Action and the reference.

For an obviousness rejection, the Examiner would have to apply the analysis of Graham v Deere, 383 US 1 (1966), relying (in this instance) upon a single prior art reference and pointing to a supposed motivation for modifying that single reference. It is respectfully submitted that this -- even if attempted by the Examiner -- remains an insufficient ground for rejection.

The Graham v Deere test for obviousness under 35 USC 103 is the subject matter of Section 2141 et seq in the Manual of Patent Examining Procedure. To briefly restate, the three inquiries, in order, are to determine the applicable prior art, then determine the differences between that art and the claimed invention, and then determine whether a person of ordinary skill in the applicable art would know to make the modification necessary to arrive at those differences in view of the prior art applied.

As has been stated by the Court of Appeals for the Federal Circuit in considering matters on appeal from the Board of Appeals within the Patent Office, obviousness is a question of law (the Court citing Graham v Deere), but this determination occurs in the context of a factual inquiry regarding the scope and content of the prior art. This factual inquiry examines what a reference would have taught or suggested to one of ordinary skill in the art at the time the of the invention (the Court citing Northern Telecom v Datapoint Corp., 908 F.2d 931, 15 USPQ2d 1321). The Court has cautioned against focusing on the obviousness of the differences between the claimed invention and the prior art rather than the obviousness of the claimed invention as a whole as 35 USC 103 requires (citing Hybritech, Inc. v Monoclonal Antibodies, Inc., 802 F.2d 1367, 231 USPQ 81) and against the use of hindsight reconstruction of what is disclosed in a prior art reference (citing Grain Processing Corp. v American Maize Products Co., 840 F.2d 902, 5 USPQ2d 1788). The Court has quoted approvingly from its decision in In re Fritch, 972 F.2d 1260, 23 USPQ2d 1780, in which it said:

> The mere fact that the prior art may [emphasis added] be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.

On the latter point, the CAFC has said that the Patent Office, in determining the obviousness of a claimed invention that combines known elements, must determine whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination (citing Lindemann Maschinenfabrik GmbH v American Hoist and Derrick Co., 730 F.2d 1452, 221 USPQ 481).

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. See In re Sernacker, 702 F.2d 989, 995; 217 USPQ 1, 6 (Fed. Cir. 1983). The reviewing court for the Patent Office requires proof by evidence in order to establish a *prima facie* case when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. See In re Knapp-Monarch Co., 296 F.2d 230, 232; 132 USPQ 6, 8 (CCPA 1961) and In re Cofer , 354 F.2d 664, 668; 148 USPQ 268, 271-272 (CCPA 1966).

No such attempt is made in the Official Action. Indeed, it is Applicants' position that no such attempt can succeed and that recognition of that failing in the prior art has resulted in the absence of any obviousness rejection from the Examiner's argument. It is submitted that this is tantamount to recognition and admission of a patentable invention as defined in the claims under consideration.

For the reasons given above, it is Applicants' position that Claim 1 defines an invention which is patentably distinct from the reference cited, whether applied or not, under the tests of both 35 USC 102 and 35 USC 103. Should the Examiner conclude otherwise, it is respectfully requested that the Examiner's arguments be clarified in any next following Official Action in order that Applicants may more clearly understand the element by element identification (if the rejection is under 35 USC 102) and/or the teaching which suggests obviousness of any combination of references (if the rejection is under 35 USC 103).

Claim 2

Claim 2 is believed to be patentable for the same reasons given above with respect to claim 1. Applicants note that claim 2 draws dependency from claim 1. Further, as established above with respect to claim 1, there is no teaching in walker of a second data input/output circuit releasing, to a data bus, data taken thereinto from a first data input/output circuit. Therefore, the following bold-highlighted portions of claim 2 distinguish over Walker:

> 2. Apparatus according to claim 1, wherein **after said second data input/output circuit outputs said data taken thereinto to said data bus**, said second data input/output circuit outputs said data thereof to said data bus.

Claim 3

Claim 3 is believed to be patentable for the same reasons given above with respect to claim 1. Although Walker contains a line coupled between input and output buffers 408 and 406, this line does not transfer data to the output buffer as required by

the following bold highlighted language expressly recited in Applicants claim 3:

> 3. Apparatus according to claim 1, wherein each of said first and second data input/output circuits includes:
>
> an output buffer for outputting data thereof;
>
> an input buffer for receiving data from the other data input/output circuit; and
>
> a relay line joining said buffers **for transferring said data to said output buffer**, said data being output from the other data input/output circuit and being received by said input buffer.

The reason is, as previously established with respect to claim 1, the value driven on to DBUS 404 by any output driver described in walker is a function only of Din. Again, see, for example, Walker's figure 3a wherein the value to be driven onto the DBUS 404 at pin 316 depends only on the value of Din 304 (and nothing else).

Claim 4

Given the above arguments, the output driver circuits in walker do not output data to Walker's data bus DBUS 404 which is data being output from the other driver circuit which is transferred from the line connecting circuits 406a and 408a (which the Examiner is trying to read as the "relay line").

This is required by the following bold highlighted language expressly recited in Applicants claim 4 and is lacking in Walker:

4. Apparatus according to claim 3, **wherein said output buffer outputs said data to said data bus, said data being output from the other data input/output circuit and being transferred from said relay line.**

In addition, Applicants incorporate by reference those arguments for patentability which were presented with respect to claim 1 and claim 3 as claim 4 depends on these claims.

Early and Favorable Notice of Allowance Requested

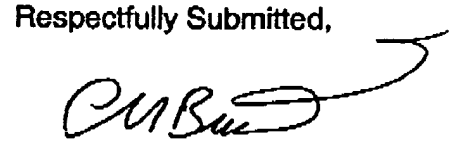
By each and all of the aforementioned and entered positions, Applicants assert that all claims stand ready for allowance as to proper form and supporting basis, and as all rejections have been traversed or rendered moot.

Applicants therefore request the Examiner remove each and all of the rejections and\or objections, and respectfully request entry of the Amendment and reconsideration of all Claims, as amended, hereunder. Applicants request an early and favorable action on the present Application and a timely Notice of Allowance.

The Examiner is invited to contact the undersigned for all issues of this Application at the telephone number and\or email address indicated below, particularly for matters that may be timely handled.

PATENT
IBM Docket No. **JP920010178US1**

Respectfully Submitted,



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